STRESS-FREE ISOLATION LAYER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to isolation techniques for semiconductor integrated circuit devices and more particularly to methods of fabricating a stress-free isolation layer for components in semiconductor integrated circuit devices.

2. Technical Background

The continuous trend of miniaturization of semiconductor devices has driven the size of integrated circuits devices into the sub-micron level. For example, more than one million components have been squeezed into a die area of less than one centimeter square for memory devices. On a chip having this level of component density, adequate isolation between neighboring components must be secured to ensure acceptable device operating characteristics. The fabrication techniques necessary for such severe isolation requirement are generally referred to as isolation techniques. The primary purpose of isolation techniques is to maintain proper isolation between components on the same chip even as the space allowed for isolation decreases because as many components as possible are placed on the chip.

In the prior art, one widely employed technique for device isolation in semiconductor chips is a technique termed "local oxidation of silicon" (also known as "LOCOS"). A thick layer of silicon dioxide formed on the chip serves the purpose of isolation to achieve effective isolation between neighboring components on a semiconductor chip. FIGS. **1A** to **1E** of the drawings show, cross sectional views, a typical device manufactured using LOCOS in various process stages of fabrication.

Referring to FIG. **1A**, a pad oxide layer **11** and a silicon nitride layer **12** are formed subsequently on a silicon substrate **10**. Microlithography and etching processes are then utilized to define required patterns on the silicon nitride layer **12**, followed by an ion implantation procedure to implant impurities in the area of the silicon substrate **10** not been covered by the silicon nitride layer **12**. A channel-stop layer **13** (as shown in FIG. **1B**) is thus formed.

In the process stage depicted by FIG. **1C**, thermal oxidation has been accomplished to form a thick layer of field oxide **14**. Due to the fact that the oxidation rate of silicon nitride is much smaller than that of silicon, the oxidation resistant silicon nitride layer **12** can be utilized as a shielding mask in the oxidation process, so that oxidation only takes place effectively in the areas of the silicon substrate **10** which have not been covered by the silicon nitride layer **12**. The formed oxidized layer is the field oxide layer **14**. Since the oxidized layer occupies more volume than the silicon used to form the layer, stress within the crystalline structure forms crystalline defects **16**. Referring to FIG. **1D**, the silicon nitride layer **12** is then removed to obtain a silicon nitride layer free configuration. Devices with acceptable isolation from each other can then be fabricated on the chip in the regions between field oxide layers **14**.

The above described prior art local oxidation or LOCOS technique suffers several drawbacks when applied to fabrication of devices having sub-micron features. First, during the process of forming the field oxide layer **14**, the oxidation not only takes place in the direction vertical to the major plane of the silicon substrate **10** but also extends in a horizontal direction. Layer **14** therefore expands into the region under the silicon nitride layer **12**. Consequently, the silicon nitride layer **12** is lifted upwards. The effect is commonly called the "birds beak" effect.

Second, the bird's beak effect results, in turn, in compression stress in the region near the surface of silicon nitride layer **12**, forcing the nitrogen-like material to diffuse into the neighboring underlying tensile-stressed pad oxide layer. The diffused nitrogen reacts with the silicon substrate **10** to form a type of nitride-like layer **15**. Because of the resistance of the nitride-like layer **15** to oxidation, this nitride-like layer **15** obstructs the subsequent growing of a gate oxide layer, acting essentially as a mask, in subsequent device fabrication procedures. As a result, the thickness in the gate oxide layer is reduced. The resulting phenomena is referred to as the "white ribbon" effect, so named because, through an optical microscope, it is observed as the apparent presence of white ribbon in the perimeter of active areas on the silicon substrate.

Third, there is a 2.2 fold volume expansion when silicon is oxidized into silicon dioxide. Therefore, the field oxide layer **14** protrudes above the surface of the silicon substrate **10**, forming a non-recessed surface.

Fourth, the channel-stop layer **13** tends to expand laterally under the influence of the high temperature and long time thermal treatment during the formation of the field oxide layer **14**, thereby narrowing the active area width. This is disadvantageous for the scaling-down of VLSI circuits.

Fifth, due to the lateral volumetric expansion of silicon during the formation of field oxide layer **14**, massive stresses result in the active area that produce crystalline defects in the bird beak regions. The crystalline defects cause an increase in junction leakage and a reduction in the reliability of the semiconductor device.

Accordingly, many new processes have been developed to overcome these drawbacks in forming isolation regions. For example, in one process, silicon dioxide sidewall spacers are formed before the formation of the field oxide layer. This is to prevent the lateral diffusion of the oxygen atoms that form the bird's beak into the silicon substrate.

Regarding the problem of the white ribbon effect, the prior art method had utilized the formation of an oxide layer on the surface of the active area. This layer and the nitride-like layer **15**, is then etched away to reveal again the surface of the device. The resulting configuration (as shown in FIG. **1E**) has a field oxide layer **14** that is partially etched away together with the nitride-like layer **15**, and is reduced in its overall thickness.

In another process buffering polysilicon (not shown) is applied between the pad oxide layer **11** and the silicon nitride layer **12**, so as to release the local stresses and minimize the amount of nitrogen diffused away. The small amount of diffused nitrogen can form a nitride-like layer in the interface between the polysilicon layer and the pad oxide layer **11**, in order to prevent the formation of white ribbons at the perimeter of active area on the silicon substrate **10**.

The top surface of a chip is preferably planar. To accomplish this a pre-etching scheme has been proposed. First, a shallow trench is formed to the depth of 2,000 to 3,000Å, then it is filled with the field oxide layer to obtain a recessed structure.

Narrowing of the active area width caused by lateral diffusion of channel-stops during high-temperature